This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An amplifier circuit comprising:

a limiter preamplifier including:

a differential amplifier coupled to receive a differential input signal at its inputs, and configured to generate a differential output signal made up of a first output signal and a second output signal, and

an output stage having a first differential output amplifier coupled to the first output signal and a second differential output amplifier coupled to the second output signal; and

a combiner distributed amplifier having a first input coupled to a first output of the first differential output amplifier, and a second input coupled to a first output of the second differential output amplifier,

wherein the output of the first differential output amplifier and the output of the second differential output amplifier are of the same phase.

2. (Original) The amplifier circuit of claim 1 further comprising:

a first level shift circuit coupled between the first output of the first differential output amplifier and the first input of the combiner distributed amplifier; and

a second level shift circuit coupled between the first output of the second differential output amplifier and the second input of the combiner distributed amplifier.

3. (Original) The amplifier circuit of claim 2 wherein the differential amplifier of the limiter preamplifier comprises a plurality of serially-coupled differential amplifier cells configured to amplify and limit a level of the differential input signal.

4. (Original) The amplifier circuit of claim 3 wherein each of the first and second level shift circuitry comprises a plurality of serially-coupled diodes.

5. (Original) The amplifier circuit of claim 1 wherein the first differential output amplifier comprises a first input coupled to the first output signal, a second input that is resistively terminated, and a second output that is 180 degrees out of phase with respect to the first output of the first differential output amplifier, the second output being resistively terminated.

6. (Original) The amplifier circuit of claim 5 wherein the second differential output amplifier comprises a first input coupled to the second output signal, a second input that is resistively terminated, and a second output that is 180 degrees out of phase with respect to the first output of the second differential output amplifier, the second output being resistively terminated.

7. (Original) The amplifier circuit of claim 1 wherein the differential amplifier comprises:

a differential input stage having first and second inputs coupled to receive the differential input signal; and

a buffer output stage coupled to the differential input stage and configured to shift a signal level at an output of the differential input stage.

8. (Original) The amplifier circuit of claim 7 wherein the buffer output stage in the differential amplifier comprises:

a first source-follower transistor coupled at a first output of the differential input stage;

a plurality of serially-coupled diodes coupled between a source terminal of the first source-follower transistor and the first output signal;

a second source-follower transistor coupled at a second output of the differential input stage; and

a plurality of serially-coupled diodes coupled between a source terminal of the second source-follower transistor and the second output signal.

9. (Original) The amplifier circuit of claim 1 wherein each of the first and the second differential output amplifiers comprises:

a first field-effect transistor having a gate terminal forming a first input node, a drain terminal forming a first output node, and a source terminal coupled to a common source node;

a second field-effect transistor having a gate terminal forming a second input node, a drain terminal forming a second output node, and a source terminal coupled to the common source node;

a first load device coupled between the first output node and a high power supply;

a second load device coupled between the second output node and the high power supply; and

a current-source device coupled between the common source node and a low power supply.

10. (Original) The amplifier circuit of claim 9 wherein each of the first and the second load device comprises a resistor coupled in series to an inductor.

11. (Original) The amplifier circuit of claim 9 wherein the first output node in each of the first and second differential amplifiers is a non-inverting node, and the second output node is an inverting node.

12. (Original) The amplifier circuit of claim 11 wherein the first input of the combiner distributed amplifier couples to the non-inverting node of the first differential output amplifier, and the second input of the combiner distributed amplifier couples to the inverting node of the second differential output amplifier.

13. (Original) The amplifier circuit of claim 12 wherein the load device coupled to the non-inverting node of the first differential output amplifier comprises a resistor coupled to an inductor, while the load device coupled to the inverting

node of the first differential output amplifier is eliminated providing for a short between the inverting node of the first differential output amplifier and the high power supply.

14. (Original) The amplifier circuit of claim 12 wherein the load device coupled to the inverting node of the second differential output amplifier comprises a resistor coupled to an inductor, while the load device coupled to the non-inverting node of the second differential output amplifier is eliminated providing for a short between the non-inverting node of the second differential output amplifier and the high power supply.

15. (Original) The amplifier circuit of claim 1 wherein the combiner distributed amplifier comprises:

a first plurality of transistor amplifier cells coupled in cascade having a common gate line coupled the first input of the combiner distributed amplifier, and a common drain line coupled to an output of the amplifier circuit; and

a second plurality of transistor amplifier cells coupled in cascade having a common gate line coupled to the second input of the combiner distributed amplifier, and a common drain line coupled to the output of the amplifier circuit.

16. (Original) The amplifier circuit of claim 15 wherein each of the transistor amplifier cells comprises a single common-source field-effect transistor.

17. (Original) The amplifier circuit of claim 15 wherein each of the transistor amplifier cells comprises a cascode-coupled pair of field-effect transistors.

18. (Original) A method of amplifying a high frequency signal comprising:

receiving a differential signal at differential inputs of a limiter circuit;

performing a limiting function on the differential signal;

using the limiter circuit to amplify the differential signal and to generate a pair of in-phase output signals; and

applying, respectively, the pair of in-phase output signals to a pair of input terminals of a combiner distributed amplifier.

19. (Original) The method of claim 18 further comprising level shifting the pair of in-phase output signal before applying them to the pair of input terminals of the combiner distributed amplifier.

20. (Currently Amended) A limiter amplifier comprising:

a differential amplifier coupled to receive a differential signal at its inputs and configured to generate a differential output signal made up of a first signal and a second signal; and

an output stage having a first differential output amplifier coupled to receive the first signal and a second differential output amplifier coupled to receive the second signal,

wherein, the first differential output amplifier comprises a first differential pair and is configured to generate a first single-ended output signal and the second differential output amplifier comprises a second differential pair and is configured to generate a second single-ended output signal that is in phase with the first single-ended output signal.

21. (Currently Amended) The limiter amplifier of claim 20 wherein the first differential output amplifier comprises a first input coupled to receive the first output signal, a second input that is resistively terminated, and a second output that is 180 degrees out of phase with respect to the first output of the first differential output amplifier, the second output being resistively terminated.

22. (Currently Amended) The limiter amplifier of claim 21 wherein the second differential output amplifier comprises a first input coupled to receive the second output signal, a second input that is resistively terminated, and a second output

that is 180 degrees out of phase with respect to the first output of the second differential output amplifier, the second output being resistively terminated.

23. (Original) The limiter amplifier of claim 20 wherein the differential amplifier comprises:

a differential input stage having first and second inputs coupled to receive the differential input signal; and

a buffer output stage coupled to the differential input stage and configured to shift a signal level at an output of the differential input stage.

24. (Original) The limiter amplifier of claim 20 wherein the differential amplifier comprises a plurality of serially-coupled differential amplifier cells configured to amplify and limit a level of the differential input signal.

25. (Original) A communication system comprising:

a receiver comprising:

an optical input circuit coupled to receive an optical signal and to convert the optical signal to an electrical signal,

a trans-impedance amplifier coupled to receive and amplify the electrical signal,

a limiter coupled to the trans-impedance amplifier; and

a demultiplexer coupled to receive an output of the limiter and configured to de-serialize the electrical signal into a plurality of lower frequency parallel signals to be transmitted to a signal processing unit; and

a transmitter comprising:

a multiplexer coupled to receive a plurality of parallel signals from the signal processing unit, and configured to serialize the parallel signals into a single differential signal;

the driver amplifier of claim 1, coupled to receive the differential signal and to generate an output signal; and

an optical modulator coupled to the driver amplifier and configured to convert the output signal into a modulated optical signal.

26. (New) The limiter amplifier of claim 20 further comprising:

a combiner distributed amplifier having a first input coupled to receive the first single-ended output signal of the first differential output amplifier, and a second input coupled to receive the second singe-ended output signal of the second differential output amplifier.

27. (New) An amplifier circuit comprising:

a first differential amplifier having a non-inverting input and an inverting input, and a non-inverting output and an inverting output;

a second differential amplifier having an input coupled to the non-inverting output of the first differential amplifier, and a non-inverting output;

a third differential amplifier having an input coupled to the inverting output of the first differential amplifier, and an inverting output;

a combiner distributed amplifier having a first input coupled to the non-inverting output of the second differential amplifier and a second input coupled to the inverting output of the third differential amplifier,

wherein the input of the second differential amplifier and the input of the third differential amplifier are the same type of input, and

wherein the first differential amplifier, the second differential amplifier, and the third differential amplifier each comprise a differential pair.

28. (New) The amplifier circuit of claim 27 wherein input of the second differential amplifier and the input of the third differential amplifier are non-inverting inputs.

29. (New) The amplifier circuit of claim 27 wherein input of the second differential amplifier and the input of the third differential amplifier are inverting inputs.